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------------  2/9/2006  10/800,196


     FILE 'CAPLUS' ENTERED AT 13:42:50 ON 09 FEB 2006
                E GUSEV I, 1996/RE
L1            2 SEA ABB=ON  PLU=ON  "GUSEV I, 1996, V278, P57, THIN SOLID
                FILMS"/RE
                D ALL 1-2

     FILE 'CAPLUS' ENTERED AT 14:16:30 ON 09 FEB 2006
                E CHIEH Y, 1992/RE
L2            5 SEA ABB=ON  PLU=ON  "CHIEH Y, 1992, V39, P1882, IEEE TRANS
                ELECTRON DEVICES"/RE
                D ALL TOT

     FILE 'STNGUIDE' ENTERED AT 14:16:46 ON 09 FEB 2006

     FILE 'SCISEARCH' ENTERED AT 14:17:29 ON 09 FEB 2006
                E CHIEH Y, 1992/RE
                E CHIEH Y S, 1992/RE
L3            0 SEA ABB=ON  PLU=ON  ("CHIEH Y S, 1992, V39, P1882, IEEE T
                ELECTRON DEV"/RE OR "CHIEH Y S, 1994, V141, P1585, J ELECTROCHE
                M SOC"/RE OR "CHIEH Y S, 1996, V17, P335, IEEE ELECT DEVICE
                LE"/RE OR "CHIEH Y S, 1996, V17, P360, IEEE ELECTR DEVICE
                L"/RE) AND TRENCH########
L4            0 SEA ABB=ON  PLU=ON  ("CHIEH Y S, 1992, V39, P1882, IEEE T
                ELECTRON DEV"/RE OR "CHIEH Y S, 1994, V141, P1585, J ELECTROCHE
                M SOC"/RE OR "CHIEH Y S, 1996, V17, P335, IEEE ELECT DEVICE
                LE"/RE OR "CHIEH Y S, 1996, V17, P360, IEEE ELECTR DEVICE
                L"/RE) AND INSULAT?
L5            0 SEA ABB=ON  PLU=ON  ("CHIEH Y S, 1992, V39, P1882, IEEE T
                ELECTRON DEV"/RE OR "CHIEH Y S, 1994, V141, P1585, J ELECTROCHE
                M SOC"/RE OR "CHIEH Y S, 1996, V17, P335, IEEE ELECT DEVICE
                LE"/RE OR "CHIEH Y S, 1996, V17, P360, IEEE ELECTR DEVICE
                L"/RE) AND FILL#######

     FILE 'HCAPLUS' ENTERED AT 14:18:42 ON 09 FEB 2006
L6        14795 SEA ABB=ON  PLU=ON  METAL#######(3A)FILL########

     FILE 'STNGUIDE' ENTERED AT 14:18:53 ON 09 FEB 2006

     FILE 'HCAPLUS' ENTERED AT 14:19:16 ON 09 FEB 2006
L7         1020 SEA ABB=ON  PLU=ON  METAL######(6A)TRENCH#######

     FILE 'HCAPLUS' ENTERED AT 14:19:26 ON 09 FEB 2006
L8         4057 SEA ABB=ON  PLU=ON  INSULAT########(6A)TRENCH#######
L9         9245 SEA ABB=ON  PLU=ON  INSULAT########(6A)FILL########
L10         216 SEA ABB=ON  PLU=ON  L7 AND L8
L11          35 SEA ABB=ON  PLU=ON  L7 AND L9
L12         920 SEA ABB=ON  PLU=ON  L8 AND L9
L13          30 SEA ABB=ON  PLU=ON  L10 AND L11 AND L12
L14       70744 SEA ABB=ON  PLU=ON  (COSI? OR TISI? OR TASI? OR NISI? OR WSI?
                OR ?SALICID? OR ?SILICID? OR ?POLYSID?)
L15           7 SEA ABB=ON  PLU=ON  L13 AND L14
                D ALL TOT
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Search Query Display

[redacted]

Recent Search Queries		**Results**
#1	((~~metal filled trench~~)<in>metadata)	0
#2	(metal filled trench<IN>metadata)	3
#3	((~~metal filled trench~~)<in>metadata)	0
#4	(metal filled trench<IN>metadata)	3
#5	(metal filled trench<IN>metadata)	3
#6	(metal filled trench<IN>metadata)	3
#7	(filled trench<IN>metadata)	37
#8	(((filled trench<in>metadata))<AND>(metal silicide<in>metadata))	0
#9	(metal silicide trench<IN>metadata)	0
#10	(metal <and> trench <and> filling <and> silicide<IN>metadata)	11
#11	(metal <and> trench <and> filling <and> silicide<IN>metadata)	11
#12	(metal silicide trench<IN>metadata)	0
#13	(metal <and> trench <and> filling <and> silicide<IN>metadata)	11

[redacted]

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Budapest Special Issue Letters Proteins and Peptides

Searched for:: :All of the words:**filling** AND **trench** AND **insulator** AND (**silicidation**)

Found:: :**39 total** | **4 journal results** | **16 preferred web results** | **19 other web results**

Sort by:: :**relevance** | date

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1. SOLID STATE IMAGING SENSOR IN A SUBMICRON TECHNOLOGY AND METHOD OF MANUFACTURING AND USE OF A SOLID STATE IMAGING SENSOR
SCHMITZ, Jurriaan / ROKS, Edwin / VERBUGT, Daniel, W., E. / KONINKLIJKE PHILIPS ELECTRONICS N.V., *PATENT COOPERATION TREATY APPLICATION*, Sep 2001
...passivating layer can contain an **insulator** material and the contact...said layer containing the **insulator** material. The radiation...conductivity type to thereby form a **trench** in said substrate **filling** the etched **trench** with a passivating material...
Full text available at patent office. For more in-depth searching go to LexisNexis
similar results

2. PROCESS FOR THE FABRICATION OF MOSFET DEPLETION DEVICES, SILICIDED SOURCE AND DRAIN JUNCTIONS
BOYD, Diane, Catherine / BRODSKY, Stephen, Bruce / HANAFI, Hussein, Ibrahim / ROY, Ronnen, Andrew / International Business Machines Corporation, *EUROPEAN PATENT*, Jun 2003
...of forming a liner and **filling** the **trench** opening with a **trench**...deposition process used in **filling** the **trench** opening also forms a...covered by oxide 32 during **silicidation**. Next, as shown in Fig. 8, an **insulator** layer 44 is formed over...
Full text available at patent office. For more in-depth searching go to LexisNexis
similar results

3. Recent applications of nuclear microprobe techniques to microelectronics
Takai, M., *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, Jul 1997
...such as SQI (Silicon-on-**Insulator**) devices for future hand-held...analyses on multi-level wiring, **silicidation** processes r4-6], and **trench filling** processes seem quite powerful...J.P. Colinge, Silicon-on-**Insulator** Technol- ogy: Materials...
Full text article available from SCIENCE DIRECT
similar results

4. Ataglan8 [PDF-296K]
May 1999
FIRST D AY AM i Session A. Semiconduc- tor Quantum Dots - Devices Room: Multicultural Center Theater 10:00 A1, Gain and Emission Characteris tics of MOVPE Grown InP/GaInP Quantum Dot Lasers .... Thomas Riedl 10:20 A2, 4 Watt High Power Quantum Dot Lasers .... M.
more hits from [http://www.tms.org/Meetings/Specialty/EMC99/EMC99-Tech...]
similar results

Did you mean?
filling trench insulator solicitation

Refine your search using these keywor found in the results
- arsenic
- chip size
- electron volts
- gate length
- implant
- impurity
- interstitials
- lithography
- metrology
- oxide layer
- point defect
- polysilicon layer
- process integration
- semiconductors
- silicide
- transistor

Or refine using:
All of the words
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filling AND elevation AND height AND trench AND insul [Search]

☑ Journal sources ☑ Preferred Web sources ☑ Other Web sources ☐ Exact phrase

Searched for:: :All of the words:**filling** AND **elevation** AND **height** AND **trench** AND **insulator** AND (**silicide**)

Found:: :**9 total** | **0 journal results** | **4 preferred web results** | **5 other web results**

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dielectric

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All of the words
[Refine]

1. Thank you for your interest in the International Technology Roadmap for Semiconductors : [PDF-930K]
Jun 2000
Welcome ! Thank you for your interest in the International Technology Roadmap for Semiconductors: 1999 edition. We have worked diligently as teams of Technology Working Groups from around the world to assess technology requirements for the semiconductor industry over the next 15 years.
[http://www.ra.informatik.uni-stuttgart.de/~rainer/Lite...]
similar results

2. DENSE ARRAYS AND CHARGE STORAGE DEVICES, AND METHODS FOR MAKING SAME
LEE, Thomas, H. / SUBRAMANIAN, Vivek / CLEEVES, James, M. / WALKER, Andrew, J. / PETTI, Christopher / KOUZNETZOV, Igor, G. / JOHNSON, Mark, G. / (...) / MATRIX SEMICONDUCTOR, INC., *PATENT COOPERATION TREATY APPLICATION*, Feb 2002
DENSE ARRAYS AND CHARGE STORAGE DEVICES, AND METHODS FOR MAKING SAME This application is a continuation-in-part of U.S. Application Serial Number 09/801,233, filed on March 6, 2001, which is a continuation- in-part of U. S.
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3. epi_fly1.p65 [PDF-2MB]
Oct 2003
DERWENT WORLD PATENTS INDEX EPI Manual Codes Part 1 © 2002 Thomson Derwent. All rights reserved Edition 6 ISBN: 1 903836 26 4 © 2002 Thomson Derwent Published by Derwent Information 14 Great Queen Street, London WC2B 5DF, United Kingdom Visit the Derwent web site at http://www.derwent.
more hits from [http://www.delphion.com/derwent/docs/EPI%20Manual%20Co...]
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4. CONTACT AND VIA STRUCTURE AND METHOD OF FABRICATION
CLEEVES, James, M. / MATRIX SEMICONDUCTOR, INC., *PATENT COOPERATION TREATY APPLICATION*, Jul 2002
...as MoW. Metal **silicides** may also be used...dielectric fill, **filling** the space between...ensure complete **filling** of the top vies...26 remains an **insulator**. Thus, by selecting...conductors at one **height** will serve as...cross-section **elevation** view of Figure...well as the fill **filling** the voids between...
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"metal filled" AND silicide [Search]

☑ Journal sources ☑ Preferred Web sources ☑ Other Web sources ☐ Exact phrase

Searched for:: :All of the words:**"metal filled"** AND **silicide**

Found:: :**51 total** | **5 journal results** | **28 preferred web results** | **18 other web results**

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Save checked results — Email checked results — Export checked results

☐ **1.** Synthesis and characterization of metal-filled carbon nanotubes by microwave plasma chemical vapor deposition
Hayashi, Y. / Tokunaga, T. / Toh, S. / Moon, W.J. / Kaneko, K., *Diamond & Related Materials*, Mar 2005
...MF-CNTs. Synthesis and characterization of **metal-filled** carbon nanotubes by microwave plasma...Abstract A new type of palladium-based **metal-filled** carbon nanotubes (MF-CNTs) was fabricated...encapsulating mechanisms. Keywords Nanotubes **Metal-filled** carbon nanofibers (MF-CNTs) Bias-enhanced...
Full text article available from SCIENCE@DIRECT
similar results

☐ **2.** METHOD FOR ENHANCING FIELD OXIDE AND INTEGRATED CIRCUIT WITH ENHANCED FIELD OXIDE
LEIBIGER, Steven, M. / HAHN, Daniel, J. / FAIRCHILD SEMICONDUCTOR CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Dec 2005
...The polysilicon tiles may be **silicided** and left electrically unconnected...spacers 60.1-60.6. There are **silicide** layers 50.1 -50. 7 on top...top of this insulator 32. **Metal filled** contact plugs 36. 1 -36.3 comlect the metal layers to the **silicide** layers on top of the source...
Full text available at patent office. For more in-depth searching go to LexisNexis
similar results

☐ **3.** Microsoft Word - Abs-temp-all.doc [PDF-704K]
May 2005
I The Nanotube (NT) Conference Series Since their conception in 1999, the NT Conferences attempt to provide an informal setting to exchange the most current information in the rapidly evolving nanotube research field.
[http://nanotube.msu.edu/nt05/abstracts/NT05-abstracts....]
similar results

☐ **4.** METHOD FOR MANUFACTURING AN ELECTRIC DEVICE WITH A LAYER OF CONDUCTIVE MATERIAL CONTACTED BY NANOWIRE
VAN SCHAIJK, Robertus, T., F. / AGARWAL, Prabhat / BAKKERS, Erik, P., A., M. / LANKHORST, Martijn, H., R. / VAN DUUREN, Michiel, J. / BALKENENDE, Abraham, R. / FEINER, Louis, F. / (...) / KONINKLIJKE PHILIPS ELECTRONICS N.V., *PATENT COOPERATION TREATY APPLICATION*, Jan 2006
...electroplating thereby forming the metallic nanowires in the pores of the membrane. The electroplating was stopped when the **metal filled** the pores. The phase change material was sputter-deposited on the superior side of the membrane so that a deposited

Refine your search using these keywor found in the results
- alloys
- carbon nanotubes
- conductive
- contact hole
- dielectric
- electron mobility
- gate leakage
- hemt structures
- insulating
- insulating layer
- metallization
- nanotubes
- nitride
- nucleation
- sapphire
- tungsten

Or refine using:
All of the words
[Refine]

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Letters Special Issue

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"metal silicide" AND trench AND (silicided OR siliciding

Search

☑ Journal sources ☑ Preferred Web sources ☑ Other Web sources ☐ Exact phrase

Searched for:: :All of the words:**"metal silicide"** AND **trench** AND (**silicided** OR **siliciding** OR **silicidation**)

Found:: :**64 total** | **6 journal results** | **47 preferred web results** | **11 other web results**

Sort by:: :**relevance** | date

Save checked results — Email checked results — Export checked results

☐ **1.** Partial silicidation method to form shallow source/drain junctions
Maa, Jer-Shen / Hsu, Sheng Teng / Peng, Chien-Hsiung / SHARP KABUSHIKI KAISHA, *EUROPEAN PATENT*, Aug 1999
...to the formation of **silicided** electrodes in active...regions of the device. **Metal-silicide** contacts are a typical...surface silicon. The **metal- silicide** is formed from a chemical...surfaces, partially **siliciding** said metal and the...metal, and completing **silicidation** at a second predetermined...MOS transistor with **silicided** source/drain electrodes...
Full text available at patent office. For more in-depth searching go to LexisNexis
similar results

☐ **2.** FABRICATION OF LATERAL RF MOS DEVICES WITH ENHANCED RF PROPERTIES
D'ANNA, Pablo, E. / XEMOD, INC., *PATENT COOPERATION TREATY APPLICATION*, Feb 2001
...resistivity per square of the **silicided** gate is significantly...interdigitated or a quasi-mesh **silicided** gate structure was...interdigitated or quasi-mesh **silicided** gate structure, wherein...layer (8) depositing a **siliciding** metal selected from...heating to form the **metal silicide** layer and (10) removing...can be fabricated. A **trench** in the epi layer is...
Full text available at patent office. For more in-depth searching go to LexisNexis
similar results

☐ **3.** TRENCH-GATE SEMICONDUCTOR DEVICES, AND THEIR MANUFACTURE
GAJDA, Mark, A. / KONINKLIJKE PHILIPS ELECTRONICS N.V., *PATENT COOPERATION TREATY APPLICATION*, Feb 2003
...comprises a **metal silicide** material. to **Trench**-gate semiconductor...upwardly from the **trench** in the form...which is of a **metal silicide** material between...surface. 5 The **metal silicide** material may...material in the **trench**, or it may...
Full text available at patent office. For more in-depth searching go to LexisNexis
similar results

☐ **4.** METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE HAVING DIFFERENT METAL SILICIDE PORTIONS
STEPHAN, Rolf / ADVANCED MICRO DEVICES, INC., *PATENT COOPERATION TREATY APPLICATION*, Sep 2003
...136 and the shallow **trench** isolations 113, 133...136 and the shallow **trench** isolations 113, 133...metal-silicon compound into a **metal silicide**. In the above example...the overlap of the **silicided** portion at a depth...barrier height of the **metal silicide** is also selected in...

Did you mean?
"metal silicide" trench (silicide OR soliciting O solicitation)

Refine your search using these keywor found in the results
- bipolar transistor
- bit line
- conductive
- dielectric layer
- emitter
- field oxide
- gate electrode
- implant
- insulating
- insulating layer
- metal layer
- mosfet
- schottky barrier
- semiconductor substra
- titanium
- titanium silicide

Or refine using:
All of the words

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"silicide trench" [Search]

☑ Journal sources ☑ Preferred Web sources ☑ Other Web sources ☐ Exact phrase

Searched for:: :All of the words:**"silicide trench"**

Found:: :**4 total** | **1 journal results** | **3 preferred web results** | **0 other web results**

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Or refine using:

All of the words

Refine

☐ **1.** TRENCH POWER MOSFET WITH PLANARIZED GATE BUS
WILLIAMS, Richard K. / CORNELL, Michael E. / CHAN, Wai Tien / ADVANCED ANALOGIC TECHNOLOGIES INC., *PATENT COOPERATION TREATY APPLICATION*, Sep 2004
Power MOSFET's and fabrication processes for power MOSFET's use a continuous conductive gate structure within trenches to avoid device topology problems caused when a gate bus extends above a substrate. The conductive gate structure forms...
Full text available at patent office. For more in-depth searching go to LexisNexis
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☐ **2.** A process simplification scheme for fabricating self-aligned silicided trench-gate power MOSFETs
Juang, M.H. / Sun, L.C. / Chen, W.T. / Ou-Yang, C.I., *Solid-State Electronics*, Jan 2001
...without degrading the device performance. In this study, a practical process scheme that fabricates self-aligned **silicide trench**-gate power MOSFETs have been proposed. By using this scheme, the masking steps for the trench-gate region and the...
Full text article available from SCIENCE DIRECT
similar results

☐ **3.** BONDED WAFER PROCESS INCORPORATING DIAMOND INSULATOR
SCHRANTZ, Gregory A. / LINN, Jack, H. / BELCHER, Richard, W. / HARRIS CORPORATION, *EUROPEAN PATENT*, Jul 1996
FIELD OF THE INVENTION The present invention relates to integrated electronic circuitry fabricated in semiconductor-on-insulator structures and, more particularly, to improved silicon-on-diamond circuits and methods of fabricating such structures....
Full text available at patent office. For more in-depth searching go to LexisNexis
similar results

☐ **4.** BONDED WAFER PROCESS INCORPORATING DIAMOND INSULATOR
SCHRANTZ, Gregory, A. / LINN, Jack, H. / BELCHER, Richard, W. / HARRIS CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Sep 1994
A semiconductor-on-insulator structure incorporating a layer of diamond material and method for preparing such. The structure comprises a layer containing diamond material and having a first surface. A layer of silicon nitride is formed on the first...
Full text available at patent office. For more in-depth searching go to LexisNexis
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trench AND filling AND (silicide OR polycide OR salicide | Search

☑ Journal sources ☑ Preferred Web sources ☑ Other Web sources ☐ Exact phrase

Searched for:: :All of the words:**trench** AND **filling** AND (**silicide** OR **polycide** OR **salicide** OR **cosi** OR **nisi** OR **tisi** OR **tasi** OR w

Found:: :**36 total** | **5 journal results** | **24 preferred web results** | **7 other web results**

Sort by:: :**relevance** | date

Save checked results | Email checked results | Export checked results

1. RIE process for etching silicon isolation trenches and polycides with vertical surfaces
Bondur, James Allan / Giammarco, Nicholas James / Hansen, Thomas Adrian / Kaplita, George Anthony / Lechaton, John S. / International Business Machines Corporation, *EUROPEAN PATENT*, Feb 1988
...including silicon bulk and **silicide** and **polycide** films to obtain vertical...film of a refractory metal **silicide**, **polycide** (**silicide**/polysilicon sandwich...to suit the particular **trench-filling** material and facilitate...
Full text available at patent office. For more in-depth searching go to LexisNexis
similar results

2. Integration challenges in sub-0.25µm CMOS-based technologies
Badenes, G. / Deferm, L., *Microelectronics Journal*, Dec 2000
...planarisation after **trench filling** if some precautions...for preventing **silicide** bridging from source...removal steps. **Silicided** n / p -type (dual...choice between **TiSi** 2 and **CoSi** 2 [24,25] . **TiSi** 2 is the standard **salicide** since at least...resistive phase of **TiSi** 2 , for highly...introduction of **CoSi** 2 in production...junctions can be **silicided** without causing...
Full text article available from SCIENCE DIRECT
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3. D:\imsi\(TF).prn.pdf [PDF-46K]
May 2002
...Line P doped poly-silicon (~900uohm-cm) Ëц **polycide** (**silicide**/poly-silicon) (**silicide** : MoSix, TaSix, WSix Ëц WSix (~80 uohm-cm...gt; HDP-CVD Process was selected as a **trench filling** oxide process in 1997. STI gap-fill process...
[http://www.postech.ac.kr/bk21/ece/Kor/Achieve/news/hyn...]
similar results

4. TRENCH MOSFET HAVING LOW GATE CHARGE
SO, Koon, Chong / GENERAL SEMICONDUCTOR, INC., *PATENT COOPERATION TREATY APPLICATION*, May 2003
...embodiments, the conductive region comprises a polycrystalline silicon portion and a refractory metal **silicide** portion (e.g., a titanium **silicide** portion). [0014] According another embodiment of the invention, a trench MOSFET device is...
Full text available at patent office. For more in-depth searching go to LexisNexis
similar results

5. WP3: Device fabrication and characterization (Workpackage leader: PA1/PA2) [26K]
Sep 2003

Did you mean?
"trench filling" (silicide polypide OR silicide OR OR nisi OR aisi OR tars wsi)

Your query was rewritt "trench filling" AND (sil OR polycide OR salicide cosi OR nisi OR tisi OR OR wsi)
We did this by adding quotes to common phr and by removing non-essential words.
- Repeat without rewi

Refine your search using these keywor found in the results
dielectric
drain region
gate length
gate oxide
mosfet
nitride
oxide layer
polysilicon
polysilicon layer
shallow trench
silicon layer
silicon substrate
step coverage
transistor
trench isolation

Or refine using:

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"6664639"	DERWENT	OR	OFF	2006/02/09 07:45
L2	1	"20010055382"	DERWENT	OR	OFF	2006/02/09 07:46
L3	1	"20010055832"	DERWENT	OR	OFF	2006/02/09 07:47
L4	1	"6440808"	DERWENT	OR	OFF	2006/02/09 07:49
L5	1	"200227799"	DERWENT	OR	OFF	2006/02/09 07:52
L6	1	"4488162"	DERWENT	OR	OFF	2006/02/09 08:08
L7	265	"10144912" "10149725" "10152911" "19511846" "19619705" "19630050" "19718721" "3736531" "4219854" "166142" "193116" "221593" "224717" "238836" "272491" "491581" "573728" "2389961" "2002238056" "2002248493" "2002258674" "2002316979" "2003220283" "699936" "9672067" "9867765" "1252915" "1258140" "1272695" "1304177" "1491483" "1533606" "1659709" "10027913" "10041749" "10150503" "10212610" "10225410" "10246175" "10297015" "19954867" "3583972" "3672450" "3673437" "3687628" "3752286" "3763608" "69207386" "1045447" "1077487" "1160855" "1187215" "1246247" "1271547" "1271652" "1342265" "1351307" "1355357" "1378060" "1390977" "1405314" "1512179" "376723" "875937" "958597" "983612" "1254972" "2271535" "4340767" "5067791" "6013627" "6188396" "7176453" "7302854" "8340057" "9120997" "10209407" "10229175" "10256510" "10313100" "11214704" "11514498" "2000019557" "2000356788" "2001085637" "2001102441" "2001135803" "2001185704" "2002016148" "2002076153" "2002198532" "2002299478" "2003007866" "2003007868" "2003007873" "2003031686" "2003068885" "2003068886" "2003078044" "2003086714"	DERWENT	OR	OFF	2006/02/09 09:05

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L12	10	L9 and trench$7	DERWENT	OR	OFF	2006/02/09 09:06
L13	3	L9 and (silicid$8 or salicid$9 or polycid$9)	DERWENT	OR	OFF	2006/02/09 09:06
L14	3	L9 and insulator	DERWENT	OR	OFF	2006/02/09 09:06
L15	5	L9 and filling	DERWENT	OR	OFF	2006/02/09 09:07
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L17	218	"2005023595" "2005085037" "2005213379" "2005280028" "4589193" "4674173" "4717682" "4725562" "4753866" "4756793" "4772569" "4824797" "4890145" "4980747" "5105253" "5338953" "5343063" "5350937" "5380672" "5386132" "5411905" "5429970" "5433794" "5455064" "5460988" "5460989" "5486714" "5508544" "5512505" "5563083" "5598367" "5633519" "5652693" "5668018" "5681776" "5707884" "5723350" "5760461" "5786612" "5847425" "5872044" "5874760" "5965913" "5990509" "6013548" "6020239" "6033957" "6034389" "6040210" "6087222" "6091102" "6096598" "6103020" "6108239" "6114205" "6124611" "6137128" "6153902" "6162658" "6207515" "6207992" "6222254" "6255158" "6255684" "6258661" "6271088" "6285073" "6300666" "6312992" "6316299" "6316309" "6342410" "6358793" "6365059" "6376312" "6387776" "6396112" "6420228" "6420239" "6429092" "6429148" "6436770" "6437383" "6437397" "6448600" "6462387" "6465836" "6479852" "6498369" "6506654" "6518614" "6518616" "6525368" "6534359" "6537860" "6537871" "6537912" "6576944" "6583466" "6590248" "6593613" "6597014" "6610566" "6624045" "6627499" "6630711" "6635525" "6646288" "6649476" "6657252" "6664161" "6667494" "6670635" "6682983" "6689650" "6689656" "6689660" "6707092" "6710418" "6717179" "6717205" "6720602" "6727544" "6734106" "6734482" "6744094" "6747305" "6759335" "6767813" "6768155" "6774426" "6777288" "6798009" "6803626" "6812092" "6815294" "6825079" "6833567" "6855603" "6870215" "6872619" "6873539" "6881627" "6897502" "6897520" "6925006" "6930918" "6933556" "6934186" "6936512" "6937516" "6946345" "6949421" "6952032" "6963103" "6969662" "6975531" "2001099158" "2002049100" "2002050896" "2002071611" "2002086904" "2002103703" "2003073511" "2003083937" "2003084863" "2003105231" "9715075" "9844561"	DERWENT	OR	OFF	2006/02/09 09:18
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L20	59	L18 and transistor$5	DERWENT	OR	OFF	2006/02/09 09:18
L21	62	L18 and trench$6	DERWENT	OR	OFF	2006/02/09 09:19
L22	15	L18 and filling	DERWENT	OR	OFF	2006/02/09 09:19
L23	19	L18 and insulator	DERWENT	OR	OFF	2006/02/09 09:19
L24	0	L18 and conductivities	DERWENT	OR	OFF	2006/02/09 09:19
L25	3	L18 and substrates	DERWENT	OR	OFF	2006/02/09 09:19
L26	110	L19 or L20 or L21 or L22 or L23 or L25	DERWENT	OR	OFF	2006/02/09 09:20

L15 ANSWER 7 OF 7 HCAPLUS COPYRIGHT 2006 ACS on STN
AN 1995:682631 HCAPLUS
DN 123:72310
ED Entered STN: 19 Jul 1995
TI MOS field-effect transistors
IN Takagi, Shinichi; Chokai, Akira
PA Tokyo Shibaura Electric Co, Japan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07030104	A2	19950131	JP 1993-169326	19930708
PRAI	JP 1993-169326		19930708		

AB Trenches are formed in doped poly-Si films and in the semiconductor substrates underneath such that the **trench** bottom becomes channel regions, **insulator** films are formed, the dopants (e.g., As) are diffused from the poly-Si films into the substrates to form source and drain regions, poly-Si is deposited and etched back to **fill** the **trenches** as gate electrodes, sidewall **insulator** films are formed in the **trenches**, and **metals** (e.g., Ti) are deposited and siliconized in self alignment. The MOSFETs have decreased parasitic resistance.

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L15 ANSWER 3 OF 7 HCAPLUS COPYRIGHT 2006 ACS on STN
AN 2003:845724 HCAPLUS
DN 140:348752
ED Entered STN: 29 Oct 2003
TI Integrating the high-voltage device and low-voltage device by using trench isolation structure
IN Lee, Tzung-Han
PA United Microelectronics Corp., Taiwan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	TW 434787	B	20010516	TW 1999-88115358	19990907
PRAI	TW 1999-88115358		19990907		

AB The present invention relates to a manufg. method to improve the short-channel effect of the trench gate, which comprises the following: providing a conductive type semiconductor substrate, and defining and etching this semiconductor substrate; forming a trench on this semiconductor substrate followed by forming a gate oxide layer on the side wall surface of the trench and the surface of the bottom; filling a polysilicon layer and a **silicide** layer into the **trench** locally, in which the polysilicon and **metal silicide** will fill the **trench** properly; forming a source/drain in the semiconductor substrate, the source/drain being located on both sides of the **trench** gate; covering the **insulating** layer on top of the **trench filled** with polysilicon layer and **metal silicide** layer; finally, making a lightly-doped drain.

US006767813B2

(12) **United States Patent**
Lee et al.

(10) **Patent No.: US 6,767,813 B2**
(45) **Date of Patent: Jul. 27, 2004**

(54) **INTEGRATED CIRCUIT DEVICES HAVING ACTIVE REGIONS WITH EXPANDED EFFECTIVE WIDTHS AND METHODS OF MANUFACTURING SAME**

(75) Inventors: **Kang-yoon Lee**, Kyungki-do (KR); **Jong-woo Park**, Seoul (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.** (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/057,745**

(22) Filed: **Oct. 26, 2001**

(65) **Prior Publication Data**

US 2002/0109182 A1 Aug. 15, 2002

(30) **Foreign Application Priority Data**

Oct. 28, 2000 (KR) 2000-63711

(51) **Int. Cl.**^{7} **H01L 21/336**

(52) **U.S. Cl.** **438/585**; 438/259; 438/296; 438/424; 438/433; 438/778

(58) **Field of Search** 438/296, 297, 438/294, 295, 259, 270, 248, 391, 589, 595

(56) **References Cited**

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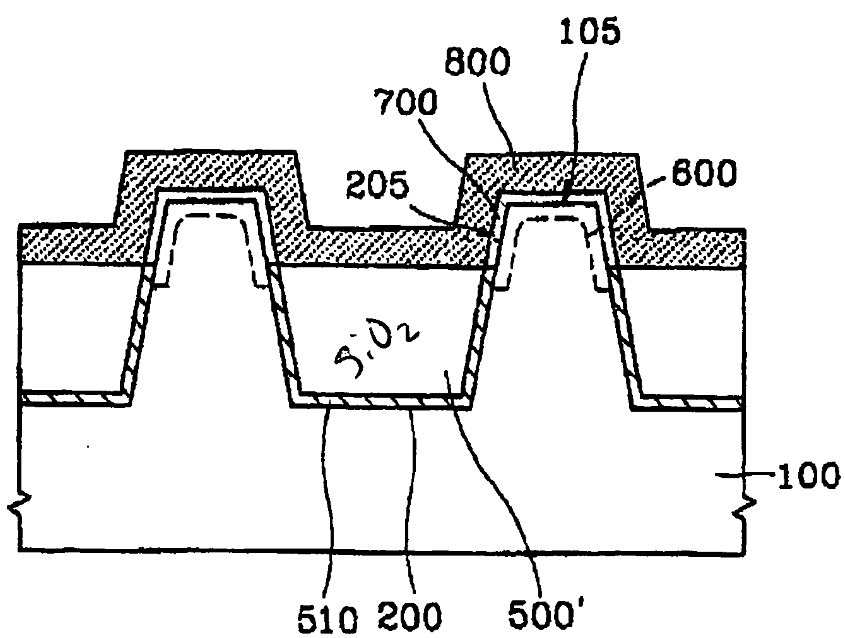
Primary Examiner—Caridad Everhart
Assistant Examiner—Chuong Anh Luu
(74) *Attorney, Agent, or Firm*—Myers Bigel Sibley & Sajovec, P.A.

(57) **ABSTRACT**

An integrated circuit device includes a substrate that has a trench formed therein. An isolation layer is disposed in the trench and covers a first sidewall portion of the trench. A gate electrode is disposed on a second sidewall portion of the trench.

24 Claims, 4 Drawing Sheets



2/9/06, EAST Version: 2.0.1.4

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L34 ANSWER 2 OF 23 WPIX COPYRIGHT 2006 THE THOMSON CORP on STN
AN 2002-265960 [31] WPIX
CR 1997-144880 [13]
DNN N2002-206532 DNC C2002-079202
TI Contact structure in integrated circuit, includes **trench isolation** region, which lies within the substrate and has trench sidewall.
IN COOPER, K J; ROTH, S S
PI US 6285073 B1 20010904 (200231)* 16 H01L029-06 <--

NOVELTY - A contact structure includes **trench isolation** region, which lies within a first portion of the substrate and has trench sidewall. A first portion of source/drain electrode abuts the trench sidewall. A portion of conductive member extends adjacent the trench sidewall, such that the first portion of the electrode is electrically shorted to the first portion of the electrode.

DETAILED DESCRIPTION - A contact structure comprises semiconductor substrate (12), **trench isolation** region, first field effect transistor (76), and conductive member. The **trench isolation** lies within a first portion of the substrate and has trench sidewall (24). The transistor has source/drain electrode lying within a second portion of the substrate. The electrode has two portions, the first portion has greater depth than that of the second portion and has less width than that of the second portion. The first portion of the electrode abuts the trench sidewall. The conductive member (64, 66) overlies the **trench isolation** region and has a portion extending adjacent the trench sidewall. The first portion of the electrode is electrically shorted to the first portion of the electrode.

USE - For use in integrated circuit.

ADVANTAGE - The horizontal surface area required to contact semiconductor devices is minimized without degrading contact resistance by utilizing the vertical surface area of the trench sidewall. The inventive contact structure allows the fabrication of integrated circuits with higher density, low contact resistance, and improved reliability.

DESCRIPTION OF DRAWING(S) - The drawing shows the cross-sectional view of the inventive contact structure.

Semiconductor substrate 12
Trench sidewall 24
Dielectric plug 34
Conductive member 64, 66
First field effect transistor 76
Second field effect transistor 78

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The conductive member further comprises second portion overlying the electrode of the transistor. The second portion is electrically shorted to a portion of the electrode abutting the major surface of the substrate. The conductive member comprises gas electrode for a second field effect transistor (78), contact plug, and laminate. The **trench isolation** region comprises dielectric plug (34). The second transistor comprises a gate electrode

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The contact plug comprises tungsten, titanium nitride, titanium **silicide,** and polysilicon. The laminate comprises **metal silicide** layer overlying a polysilicon layer. The dielectric plug comprises silicon dioxide and silicon nitride. The gate electrode comprises polysilicon layer.

L34 ANSWER 15 OF 23 EPFULL COPYRIGHT 2006 EPO/FIZ KA on STN

AN 1994:13657 EPFULL
DUPD 20040121 DUPW 200404
TIEN Method of formation of a **trench isolation** structure in an integrated circuit.
PI **EP 646956** **B1 20030129**
PRAI US 1993-130052 A 19930930
ABEN
The reliability of integrated circuits fabricated with **trench isolation** is improved by increasing the thickness of the gate dielectric overlying the **trench** corner. After the **trench isolation** region (40, 56) has been formed a thin layer of silicon dioxide (44) is chemically vapor deposited over the **trench isolation** region (44) and the adjacent active region (23). A transistor gate electrode (46) is subsequently formed over the thin layer of silicon dioxide (44). The thin layer of silicon dioxide (44) increases the thickness of the gate dielectric that lies between the transistor gate electrode (46) and the trench corner, and therefore the breakdown voltage of the gate dielectric at the trench corner is increased.

DETDEN . . .
In FIG. 9, a second dielectric layer 44 is then formed overlying first dielectric layer 42, active region 23, and **trench isolation** region 40. In addition, second dielectric layer 44 and first dielectric layer 42 have a combined thickness of less than. . . two times the thickness of second dielectric layer 44. This is because the area between the trench plug and the **trench** corner is **filled** or plugged by second dielectric layer 44. Therefore, the breakdown voltage of the gate dielectric lying between the trench corner. . . increased. In a preferred embodiment first transistor gate electrode 46 comprises polysilicon. Alternatively, transistor gate electrode 36 may be a **metal**, a **metal silicide**, a **metal** nitride, or a composite of polysilicon and a metal, or a composite of polysilicon and a **metal silicide**, or a composite of polysilicon and a metal nitride. As shown in FIG. 9, transistor gate electrode 46 overlies second deposited dielectric layer 44, active region 23, and **trench isolation** region 40.
DETDEN
[0011] In FIG. 5, a **trench fill** material 32 is then formed overlying etch stop layer 16 and trench liner 28, such that **trench** 22 is substantially **filled**. In a preferred embodiment, **trench fill** material 32 is chemically vapor deposited silicon dioxide, which is deposited using ozone and tetraethylorthosilicate (TEOS) as source gases. Alternatively, **trench fill** material 32 may also be another dielectric material, such as germanium oxide, spin-on-glass, et cetera, or a combination of different materials such as polysilicon and silicon dioxide. In addition, **trench fill** material 32 may be formed using other techniques such as plasma enhanced chemical vapor deposition, electron cyclotron resonance deposition, or. . .

US006222254B1

(12) United States Patent
Liang et al.

(10) **Patent No.:** **US 6,222,254 B1**

(45) **Date of Patent:** ***Apr. 24, 2001**

(54) **THERMAL CONDUCTING TRENCH IN A SEMICONDUCTOR STRUCTURE AND METHOD FOR FORMING THE SAME**

(75) Inventors: **Chunlin Liang**, San Jose; **Brian S. Doyle**, Cupertino, both of CA (US)

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **08/829,860**

(22) Filed: **Mar. 31, 1997**

(51) **Int. Cl.**[7] **H01L 29/72**; H01L 29/30

(52) **U.S. Cl.** **257/622**; 257/401; 257/399; 257/408; 257/9; 257/327

(58) **Field of Search** 257/622, 399, 257/714, 280, 327, 347, 733, 9, 300–305, 296, 330–334, 401, 408

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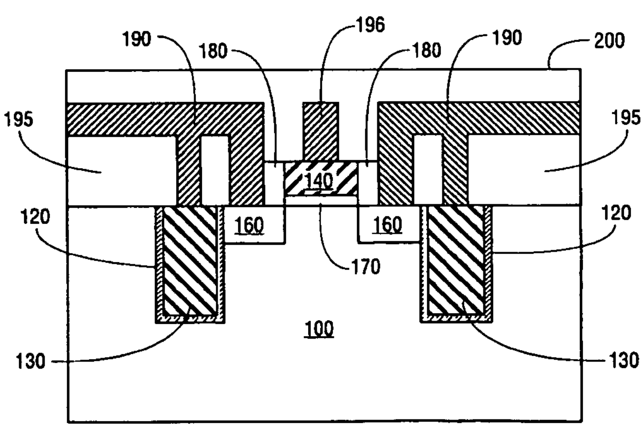
Primary Examiner—Alexander O. Williams
(74) *Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman LLP

(57) **ABSTRACT**

The invention relates to a method of forming a trench filled with a thermally conducting material in a semiconductor substrate. In one embodiment, the method includes filling a portion of the trench with a thermally conducting material and patterning a contact to the thermally conducting material. The invention also relates to a semiconductor device. In one embodiment, the semiconductor device has a trench defining a cell region, wherein a portion of the trench includes a thermally conducting material, and a contact to the thermally conducting material. The invention further relates to a semiconductor device and a method of forming a semiconductor device with an interlayer dielectric that is a thermally conducting material.

12 Claims, 8 Drawing Sheets



elements of various active. . .

L34 ANSWER 19 OF 23 EPFULL COPYRIGHT 2006 EPO/FIZ KA on STN

AN 1985:6697 EPFULL
DUPD 19920826 DUPW 199235

TIEN Method of selectively exposing the sidewalls of a trench and its use to the forming of a **metal silicide** substrate contact for dielectric **filled** deep **trench isolated** devices.

PI **EP 166983** **B1 19920826**

PRAI US 1984-626271 A 19840629

ABEN

Deep trenches (14, 15) are formed according to the desired pattern through the N epitaxial layer (13) and N+ subcollector region (12) into the P- substrate (11) of a silicon structure (10). Where a substrate contact is needed, the trenches delineate a central stud (16) or mesa of silicon material. Channel stop regions (18) are formed e.g. by ion implantation of boron atoms at the bottom of trenches. SiO_2 and Si_3N_4 layers (17, 19) are then deposited on the whole structure. A substrate contact mask is applied end patterned to selectively expose one side of the trench sidewalls, the bottom of the trenches adjacent thereto and others areas if desired such as the top surface of the stud. The composite SiO_2/Si_3N_4 layer is then etched to leave exposed only the sidewalls of the stud, et least partially the bottom of the trenches adjacent thereto and the top surface of the stud. Platinum is deposited preferably via sputter deposition, conformally coating all regions of the structure. After sintering, the unreacted platinum is removed using wet chemical etch (aqua regia). Platinum silicide is left in all opened contacts and on the stud sidewalls where its defines a **metal silicide** lining (25) or **cap**, covering the stud. This lining connects the top surface (25a) of the stud, with the channel stop implanted regions (18) and thence forms the desired substrate contact.

17.The process of claim 16 further comprising the steps of :

blanket depositing a layer (25) of a **silicide** forming **metal**;

sintering the structure to produce **metal silicide** wherever said **metal** contacts silicon; and,

removing the unreacted **metal**, leaving a **metal silicide cap** covering the stud and channel stopper regions, therefore providing an electrical contact between the top side of the structure and. . .

20.The process of claim 19 further comprising the step of **filling** the **trenches** with polyimide and **reactively** ion etching in an O2 plasma the polyimide in excess to let exposed the **top** part of said **metal silicide cap** to be used as a substrate contact.

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L34 ANSWER 20 OF 23 EPFULL COPYRIGHT 2006 EPO/FIZ KA on STN

U.S. 4,589,193

AN 1985:5607 EPFULL
DUPD 19910904 DUPW 199136

TIEN **Metal silicide** channel stoppers for integrated circuits and method for making the same.

PI **EP 166142** **B1 19910904**

PRAI US 1984-626278 A 19840629

ABEN

Disclosed is the use of **metal silicide** (e.g. Pt-Si) contacts in boron lightly doped P- type silicon between two contiguous but not adjacent N+ type regions instead of employing the usual P+ implanted or diffused channel stoppers. The invention finds a particularly interesting application in polyimide **filled** deep **trench** **isolated** integrated circuits.

CLMEN . . . of said insulating layer (20) from the bottom of said trench; and,

forming a channel stopper (22a) consisting of a **metal** **silicide** rectifying contact of an appropriate **metal** at the bottom of said trench where said material was removed.

7.. . . composite insulating layer formed on the sidewalls of the said trench; said structure characterized in that it further includes a **metal silicide** rectifying contact in intimate contact with said exposed portion of said substrate.

8.The semiconductor structure of claim 7 wherein the thickness of said **metal silicide** rectifying contact is in the 50-150 nm range.

United States Patent [19]
El-Kareh et al.

[11] **Patent Number:** **4,725,562**
[45] **Date of Patent:** **Feb. 16, 1988**

[54] **METHOD OF MAKING A CONTACT TO A TRENCH ISOLATED DEVICE**

[75] Inventors: **Badih El-Kareh**, South Hero; **Richard R. Garnache**, Shelburne, both of Vt.; **Ashwin K. Ghatalia**, Hopewell Junction, N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **844,655**

[22] Filed: **Mar. 27, 1986**

[51] **Int. Cl.**[4] **H01L 21/302**
[52] **U.S. Cl.** **437/67**; 437/33; 437/225; 437/187; 437/235
[58] **Field of Search** .... 29/576 W; 156/659.1, 156/652, 661.1, 643; 148/DIG. 75, DIG. 50

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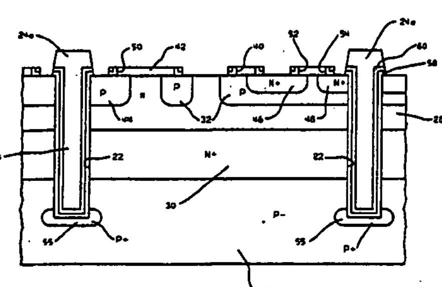
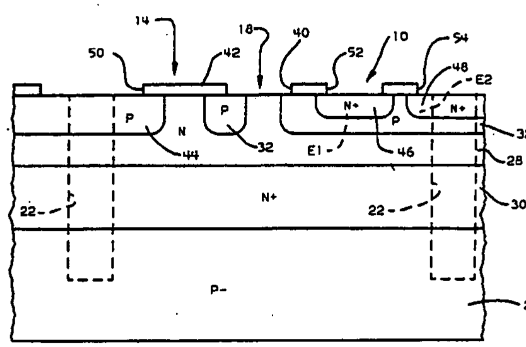
Primary Examiner—Brian E. Hearn
Assistant Examiner—Kevin McAndrews
Attorney, Agent, or Firm—Stephen J. Limanek

[57] **ABSTRACT**

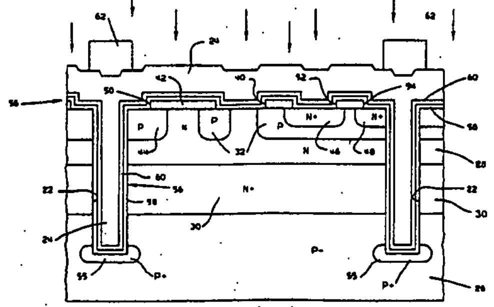
A method or process is provided for making a semiconductor structure which includes the steps of forming in a semiconductor body a P/N junction and an opening in an insulating layer disposed on the surface of the semiconductor body. A trench is then formed in the semiconductor layer having a sidewall located along a given plane through the opening and through the P/N junction. An insulating material is disposed within the trench and over the insulating layer and a block or segment of material is located over the trench so as to extend a given distance from the trench over the upper surface of the body. The insulating material and the block are then etched so as to remove the block and the insulating material located along the sides of the block. A layer of low viscosity material is formed over the semiconductor body so as to cover the remaining portion of the insulating material, the layer of low viscosity material and the insulating material having similar etch rates. The layer of low viscosity material and the insulating material are then simultaneously etched directionally until all of the layer of low viscosity material is removed. Metallic contacts may now be formed on the surface of the semiconductor body without the concern that the metallic material will seep or enter into the trench causing a short at the P/N junction.

20 Claims, 9 Drawing Figures

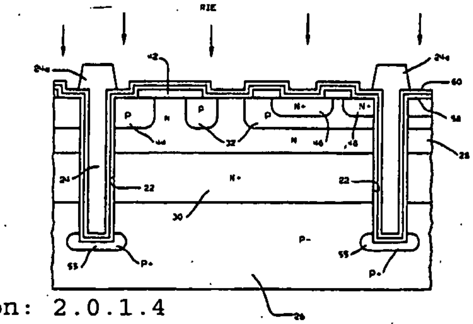




RIE



RIE



United States Patent [19]

Taka et al.

[11] Patent Number: 4,717,682

[45] Date of Patent: Jan. 5, 1988

[54] METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH CONDUCTIVE TRENCH SIDEWALLS

[75] Inventors: Shin-ichi Taka; Jiro Ohshima, both of Kawasaki; Masahiro Abe, Yokohama; Masaharu Aoyama, Fujisawa, all of Japan

[73] Assignee: Kabushiki Kaisha Toshiba, Kawasaki, Japan

[21] Appl. No.: 830,928

[22] Filed: Feb. 19, 1986

[30] Foreign Application Priority Data

Feb. 20, 1985 [JP] Japan 60-30576

[51] Int. Cl.⁴ H01L 21/283

[52] U.S. Cl. 437/31; 437/67; 437/233; 437/203; 357/34; 357/59

[58] Field of Search .... 29/591; 357/22 K, 68, 357/59 K, 59 H, 59 I, 34; 156/657, 653, 643

[56] References Cited

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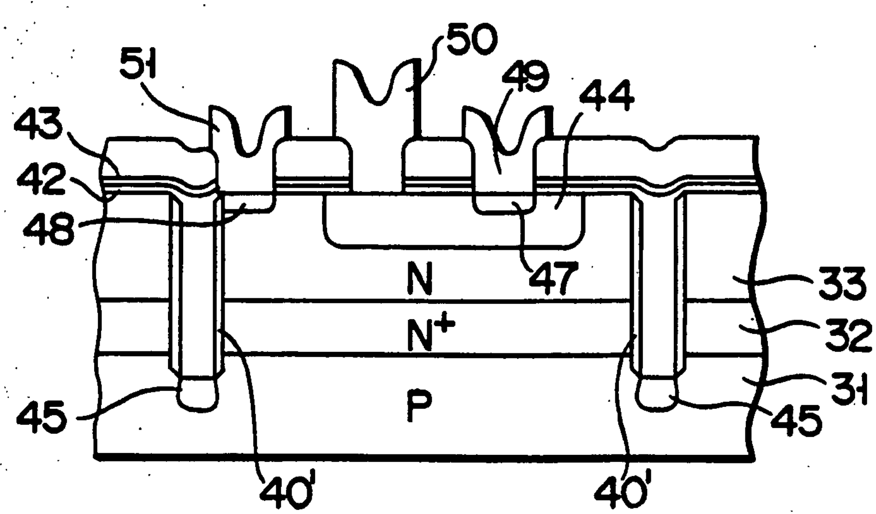
Primary Examiner—Brian E. Hearn
Assistant Examiner—Kevin McAndrews
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner

[57] ABSTRACT

A method of manufacturing a semiconductor device, comprising the steps of sequentially forming a buried region and an epitaxial layer on a major surface of a semiconductor substrate, forming a conductive layer along an annular trench extending to the buried region, filling the annular trench with an insulating material and forming a functional element in said epitaxial layer surrounded by said buried region and said insulating material within said annular trench. In this method, the step of forming the conductive layer along the annular trench is carried out by the steps of forming an annular trench extending through said buried region, and depositing a conductive layer on only a side wall surface of said annular trench.

5 Claims, 14 Drawing Figures



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L34  ANSWER 6 OF 23  WPIX  COPYRIGHT 2006 THE THOMSON CORP on STN
AN   1987-359331 [51]   WPIX
DNN  N1988-027740        DNC C1988-016303
TI   Semiconductor device mfr., esp. recessed gate device - by forming grooves
     and forming silicide metallisation in the groove bottoms.
DC   L03 U11 U12 U13
PA   (SYLV) GTE LAB LTD
CYC  2
PI   JP 62262468      A  19871114 (198751)*       9                    <--
     US 4713358       A  19871215 (198806)                             <--
ADT  JP 62262468 A JP 1987-106501 19870501; US 4713358 A US 1986-858762
     19860502
PRAI US 1986-858762       19860502
IC   H01L021-28; H01L029-80
AB   JP  62262468 A UPAB: 19930922
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Semiconductor device, esp. a recessed gate static induction transistor is formed by: forming a low resistivity layer of first type an a high resistivity epitaxial layer of first type grown on a low resistivity Si substrate of first type; etching parallel grooves (20) through the low resistivity layer into the epitocial layer; implanting zones (30) of second type at the bottoms of the grooves; forming oxide (33) on the groove sidewalls leaving exposed Si at the groove bottoms and ridge surfaces; depositing a **silicide**-forming **metal** (35); rapidly annealing to form **silicide** (35A) at the Si surfaces; and removing unreacted **metal** from the non-**silicide** areas.

ADVANTAGE - Method overcomes prior art difficulty of providing good groove bottoms metallisation while leaving no metal an the groove sidewalls. (First major country equivalent to J62262468-A)

7/8

ABEQ US 4713358 A UPAB: 19930922

Semiconductor device, esp. a recessed gate static induction transistor is formed by: forming a low resistivity layer of first type an a high resistivity epitaxial layer of first type grown on a low resistivity Si substrate of first type; etching parallel grooves (20) through the low resistivity layer into the epitocial layer; implanting zones (30) of second type at the bottoms of the grooves; forming oxide (33) on the groove sidewalls leaving exposed Si at the groove bottoms and ridge surfaces; depositing a **silicide**-forming **metal** (35); rapidly annealing to form **silicide** (35A) at the Si surfaces; and removing unreacted **metal** from the non-**silicide** areas.

ADVANTAGE - Method overcomes prior art difficulty of providing good groove bottoms metallisation while leaving no metal an the groove sidewalls. (First major country equivalent to J62262468-A)

United States Patent [19]
Goth et al.

[11] Patent Number: 4,589,193

[45] Date of Patent: May 20, 1986

[54] **METAL SILICIDE CHANNEL STOPPERS FOR INTEGRATED CIRCUITS AND METHOD FOR MAKING THE SAME**

[75] Inventors: George R. Goth; Thomas A. Hansen; Robert T. Villetto, Jr., all of Poughkeepsie, N.Y.

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: 626,278

[22] Filed: Jun. 29, 1984

[51] Int. Cl.⁴ H01L 21/76; H01L 21/94

[52] U.S. Cl. .... 29/576 W; 29/578; 29/580; 148/DIG. 19; 148/DIG. 85; 148/DIG. 86; 357/49

[58] Field of Search .... 29/576 W, 580, 578; 148/DIG. 19, 147, 50, 117, DIG. 85; 427/88; 357/49, 67 S

[56] **References Cited**

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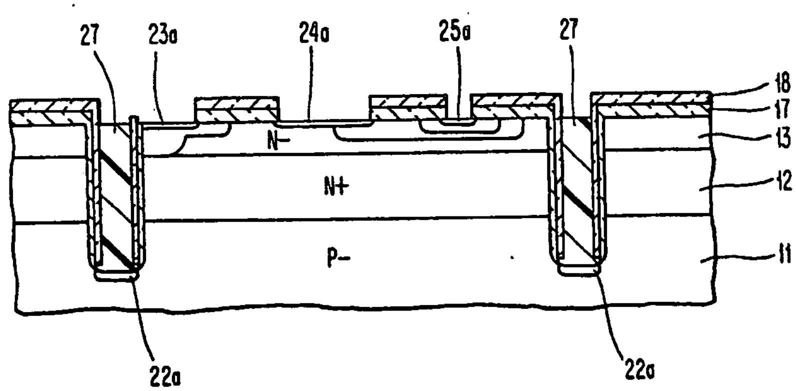
Primary Examiner—Brian E. Hearn
Assistant Examiner—Hunter L. Auyang
Attorney, Agent, or Firm—Robert J. Haase

[57] **ABSTRACT**

Disclosed is the use of metal silicide (e.g. Pt-Si) contacts in boron lightly doped P− type silicon between two contiguous but not adjacent N+ type regions instead of employing the usual P+ implanted or diffused channel stoppers. The invention finds a particularly interesting application in polyimide filled deep trench isolated integrated circuits.

The trench sidewalls are coated with an insulating material which is removed from the trench bottom at the all contact etch step. The Pt-Si is formed at the bottom of the trenches at the same time that the device contacts are made.

12 Claims, 9 Drawing Figures



L28 ANSWER 12 OF 24 WPIX COPYRIGHT 2006 THE THOMSON CORP on STN
AN 2004-338020 [31] WPIX
DNC C2004-128329
TI Method for fabricating heterojunction bipolar transistor.
DC L03 U11 U12 U13
IN CHA, H S
PA (HYNI-N) HYNIX SEMICONDUCTOR INC
CYC 1
PI KR 2003092528 A 20031206 (200431)* 1 H01L029-737
ADT KR 2003092528 A KR 2002-30221 20020530
PRAI KR 2002-30221 20020530
IC ICM H01L029-737
AB KR2003092528 A UPAB: 20040514

NOVELTY - A method for fabricating a heterojunction bipolar transistor (HBT) is provided to easily fabricate a bipolar complementary metal oxide semiconductor (BiCMOS) device employing CMOS and HBT by simplifying the process for forming a silicon germanium HBT and by simultaneously embodying the CMOS and the HBT

DETAILED DESCRIPTION - An N+ silicon epi-layer (22) and an N-silicon epi-layer (23) are sequentially grown on a substrate (21). The N-silicon epi-layer, the N+ silicon epi-layer and the substrate are etched to form a first **trench**. Silicon is **filled** in the first **trench**. Predetermined portions of the N-silicon epi-layer including the first trench portion are etched to form the second **trenches**. An **oxide** layer is **filled** in the second **trenches**. An ion implantation mask exposing a collector formation region is formed on the N-silicon epi-layer. N-type impurity ions are implanted into the exposed region to form a collector region (27). A silicon germanium (SiGe) layer (28) and a silicon epi-layer (29) are sequentially formed on the exposed N- silicon epi-layer region except the collector region. A polysilicon layer (30) and a tetraethoxysilane (TEOS) layer are sequentially formed. The TEOS layer, the polysilicon layer, the silicon epi-layer and the SiGe layer are patterned to form an emitter (32) on the **N**- silicon epi-layer region. **P**-type impurity ions are implanted into the **N**-silicon epi-layer region at both sides of the emitter to form a base region (34). The TEOS layer is removed and a spacer is formed on both **sidewalls** of the emitter. Metal **silicide** (36) is formed on the collector region, the base region and the emitter.

Dwg.1/10

L28 ANSWER 14 OF 24 WPIX COPYRIGHT 2006 THE THOMSON CORP on STN
AN 2003-626462 [59] WPIX
DNN N2003-498528 DNC C2003-171192
TI Photodetector, useful for optical communications, comprises buried insulator formed on substrate, buried mirror on the buried insulator, semiconductor-on-insulator layer, and backside contact to one of **n** -type and **p**-type doped fingers.
DC L03 U13
IN COHEN, G M; RIM, K; ROGERS, D L; SCHAUB, J D; YANG, M
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 2003122210 A1 20030703 (200359)* 25 H01L031-06
US 6667528 B2 20031223 (200408) H01L031-058

NOVELTY - Photodetector comprises:

(a) a buried insulator formed on a semiconductor substrate;

(b) a buried mirror on the buried insulator;

(c) a semiconductor-on-insulator (SOI) layer formed on the conductor;

(d) alternating **n**-type and **p**-type doped fingers formed in the SOI layer; and

(e) a backside contact to one of the **n**-type and **p** -type doped fingers.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(a) a method of forming a photodetector, which comprises forming a wafer with a buried mirror and a buried **oxide**; etching **trenches** in the wafer; **filling trenches** with a sacrificial dopant source material of a first type; etching the dopant source material of the first type from a portion of the **trenches** ; **filling** the portion of the **trenches** with a sacrificial dopant material of a second type; diffusing dopant from the sacrificial dopant material of the first type into trench walls to form a junction of the first type and diffusing dopant from the sacrificial dopant material of the second type into trench walls to form a junction of the second type; etching the sacrificial material from all of the trenches; **siliciding walls** of the trenches; forming metal plugs in the trenches; and providing separate contacts to a first set of trenches and a second set of trenches;

(b) a chip comprising a chip substrate and a photodetector formed on the chip substrate; and

(c) an optoelectronic device comprising a substrate having a via for alignment of a fiber to it.

USE - The photodetector is useful for optical communications, particularly in a complementary metal oxide semiconductor (CMOS) chip, a bipolar chip or a bipolar CMOS chip (Claimed).

ADVANTAGE - The photodetector is compatible with silicon processing. It has a reduced junction capacitance and lower series resistance, exhibits a higher quantum efficiency and allows efficient coupling of an optical fiber.

DESCRIPTION OF DRAWING(S) - The figure illustrates a semiconductor-on-**insulator trench** detector with a buried mirror and a backside contact.

Dwg.3a/12

TECH US 2003122210 A1UPTX: 20030915

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The SOI comprises silicon-on-insulator. The mirror comprises metal or a dielectric stack. It is corrugated at a surface adjacent the buried insulator. The fingers include a portion formed of silicide. The fingers comprise alternating **p**-type and **n**-type doped silicon, two silicide films respectively formed adjacent the alternating **p**-type and **n**-type doped silicon, and a metal plug formed adjacent the silicide films. The photodetector further comprises a second buried insulator formed on the mirror.

L28 ANSWER 16 OF 24 WPIX COPYRIGHT 2006 THE THOMSON CORP on STN
AN 2003-182195 [18] WPIX
DNN N2003-143329 DNC C2003-047913
TI Manufacture of vertical power metal oxide semiconductor field effect transistor involves introducing sidewall doping process.
DC L03 U11 U12
IN TSUI, B
PA (EPIS-N) EPISIL TECHNOLOGIES INC
CYC 1
PI US 6489204 B1 20021203 (200318)* 10 H01L021-336
ADT US 6489204 B1 US 2001-932727 20010820
PRAI US 2001-932727 20010820
IC ICM H01L021-336
AB US 6489204 B UPAB: 20030317

NOVELTY - A vertical power metal oxide semiconductor field effect transistor (MOSFET) is made by forming a silicon oxide layer on polysilicon exposed sidewalls, forming an N+ source area through ion implantation by an ion beam, forming **insulating** spacers on **trench** walls, implanting acceptor ions, and forming a silicide contact to the polysilicon and a single silide contact.

DETAILED DESCRIPTION - Manufacture of a vertical power MOSFET comprises:

(i) providing a silicon wafer having an N+ bottom layer (11), an **N** type middle layer (12), and a **P** body (13) top layer having an upper surface;

(ii) forming a pad oxide layer (14) on the P body top layer, and depositing a silicon nitride layer;

(iii) patterning the silicon nitride and pad oxide layers to form a mask that defines a trench, having a floor and sidewalls, and then etching the trench to a depth to extend into the N type middle layer;

(iv) forming a first silicon oxide layer (21) on the floor and sidewalls;

(v) overfilling the trench with polysilicon and etching back the polysilicon (22) until it under-**fills** the **trench**;

(vi) removing from the sidewalls all exposed silicon oxide;

(vii) forming a second layer of silicon oxide on the polysilicon exposed sidewalls, where all polysilicon in the trench is encapsulated in a silicon oxide layer;

(viii) forming an N+ source area (51) through ion implantation by an ion beam, part of which overlaps and abuts the polysilicon encapsulating oxide layer then removing the silicon nitride layer (15);

(ix) depositing a conformal layer of a dielectric material and selectively removing all dielectric material on horizontal surfaces where insulating spacers (71) on the walls of the trench are formed;

(x) implanting acceptor ions to form a **P**+ region that abuts the **N**+ source area; and

(xi) forming a silicide contact (91) to the polysilicon and a single silide contact to both the **N**+ source area and to the **P** + region.

USE - For manufacturing a vertical power MOSFET used in power electronics systems.

ADVANTAGE - The method provides a MOSFET having higher cell density, higher speed, easy scalability, and wide application. It reduces the source width, minimizes gate resistance, and minimizes the contact number and contact resistance. The sidewall doping process eliminates the need for a source implantation mask while the **sidewall** spacer facilitates **silicide** formation at the source, P body contact, and polysilicon gate, simultaneously.

DESCRIPTION OF DRAWING(S) - The figures show part of the polysilicon removed, the structure at the completion of source formation, and the completed device with silicide contacts.

N+ bottom layer 11

------------ 2/9/2006 10/800,196

N type middle layer 12
P body 13
Pad oxide layer 14
Silicon nitride layer 15
Silicon oxide layer 21
Polysilicon 22
N+ source area 51
Spacers 71
Silicide contact 91
3, 6, 9/9

TECH US 6489204 B1 UPTX: 20030317

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Process: The ion beam is directed at the silicon wafer at 30-60degrees while the wafer rotates relative to the beam. The ion beam is arsenic ions having an energy of 30-80 kV, and deposited to achieve a concentration of 5x1019-5x1020 ions/cc. The overfilling step is replaced by overfilling the trench with polysilicon, then planarizing the wafer until there is no polysilicon outside the trench, and then removing polysilicon from the trench by reactive ion etching or chemical etching. A punch through implantation is added after step of depositing a conformal layer and before step of implanting acceptor, thus enabling source to source spacing to be reduced. Preferred Component: The insulating spacers extend upwards from the polysilicon as far the upper surface of the wafer, or as far as 0.1-0.3mum below the upper surface of the wafer.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The dielectric material is silicon oxide or silicon nitride. The silicide contact is titanium silicide, cobalt silicide, or nickel silicide. The diffusion source is phosphorus oxychloride gas.

TECHNOLOGY FOCUS - CERAMICS AND GLASS - Preferred Component: The diffusion source is a layer of glass from phosphosilicate glass or arsenosilicate glass.